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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,994	02/09/2004	J. Orion Pritchard	ALTRP115	9088

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EXAMINER	
CERULLO, JEREMY S	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,994	PRITCHARD ET AL.	
	Examiner	Art Unit	
	Jeremy S. Cerullo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-20 and 22-30* is/are rejected.

7)☒ Claim(s) *5 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20050606*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending in the following action.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 14 recites the limitation "the primary component fabric" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 3-5, 7, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0199741 ("Floman") in view of U.S. Patent No. 5,623,645 ("Yip" et al.).

8. As for Claim 1, Floman teaches a memory controller with a plurality of signal pins (lines) operable to allow access to off-chip devices, wherein the memory controller is configured to use separate signal pins to access different off-chip devices (Figures 1 and 4; Page 3, Paragraphs [0031]-[0033] and [0039]). While Floman does not explicitly teach that a processor is also included on the chip, Floman does teach that the memory controller (ASIC) is used to communicate between a processor and memory (Page 1, Paragraph [0004]). However, Yip teaches a system on a chip that includes both a memory controller and a processor (Figure 3). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included a processor as taught by Yip on the chip as taught by Floman in order to simplify the computer system by reducing separate components.

9. As for Claim 3, Floman also teaches the limitation that separate control lines are always maintained.

10. As for Claim 4, it is inherent that a processor is a state machine.

11. As for Claim 5, Floman and Yip do not teach configuring the hardware circuit using a graphical user interface. OFFICIAL NOTICE is taken that hardware is routinely configured under a graphical user interface such as Windows 95/XP through such items as the registry or control panel. It would have been obvious to one of ordinary skill in the art at the time of the invention to have configured the controller of Floman and Yip using a graphical user interface in order to make configuration intuitive.

12. As for Claim 7, the examiner takes OFFICIAL NOTICE that SDRAM and SRAM are common tri-state devices accessible by a memory controller, and as such It would have been obvious to one of ordinary skill in the art at the time of the invention to have included them in the tri-state devices accessible by the memory controller of Floman and Yip.

13. As for Claim 16, it is inherent that for a memory controller to access a memory, there is a logic circuit determining which memory is to be accessed.

14. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Floman and Yip as applied to claim 1 above, and further in view of U.S. Patent No. 4,644,494 ("Muller"). Floman and Yip teach all of the limitations inherited from Claim 1, but they do not teach the use of shared address and data lines (Column 8, Lines 44-56). However, Muller teaches a system in which the address and data signals can be sent on shared lines. It would have been obvious to one of ordinary skill in the art at the time of the

invention to have used the shared lines taught by Muller in the system of Floman and Yip in order to simplify the circuit by reducing signal lines.

15. Claims 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Floman and Yip as applied to claim 1 above, and further in view of U.S. Patent No. 6,801,459 ("Riesenman" et al.).

16. As for Claim 6, Floman and Yip teach all of the limitations inherited from Claim 1, but they do not teach that the I/O lines comprise data mask lines. However, Riesenman teaches that a set of signals transmitted by a memory controller comprises data-masking signals (Column 3, Lines 36-54). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included these signals in the signal lines of Floman and Yip in order to increase the functionality of the system.

17. As for Claim 15, Floman and Yip teach all of the limitations inherited from Claim 1, but they do not teach that the I/O lines comprise address, data, mask, and control lines. However, Riesenman teaches that a set of signals transmitted by a memory controller comprises data-masking signals (Column 3, Lines 36-54). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included these signals in the signal lines of Floman and Yip in order to increase the functionality of the system.

18. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Floman and Yip as applied to claims 1 and 7 above, and further in view of U.S. Patent No. 5,875,470 ("Dreibelbis" et al.).

19. As for Claim 8, Floman and Yip teach all of the limitations inherited from Claims 1 and 7, but they do not teach that the SDRAM is arranged in multiple banks with independent row address management. However Dreibelbis does teach the use of multiple banks of SDRAM with independent row addressing. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the addressing as taught by Dreibelbis in the system of Floman and Yip.

20. As for Claims 9-10, the limitations of the claims describe a burst transaction, which is taught by Dreibelbis in Column 10, Lines 40-61.

21. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Floman and Yip as applied to claim 1 above, and further in view of U.S. Patent No. 6,836,815 ("Purcell" et al.)

22. As for Claims 11-12, Floman and Yip teach all of the limitations inherited from Claim 1, but they do not teach the use of a simultaneous multiple primary component fabric coupling the processor core to the memory controller, allowing separate primary components to access separate secondary components concurrently. However, Purcell teaches the use of a crossbar switch network, that allows separate processors to access separate memory controllers (Figure 1; Abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included such a

network in the system of Floman and Yip in order to increase the efficiency of the system.

23. As for Claim 13, the examiner takes OFFICIAL NOTICE that multiplexers are a common component of crossbar switch networks.

24. Claims 17, 19-21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0199741 ("Floman") in view of U.S. Patent No. 5,623,645 ("Yip" et al.).

25. As for Claim 17, Floman teaches a memory controller with a plurality of signal pins (lines) operable to allow access to off-chip devices, wherein the memory controller is configured to use separate signal pins to access different off-chip devices (Figures 1 and 4; Page 3, Paragraphs [0031]-[0033] and [0039]). While Floman does not explicitly teach that a processor is also included on the chip, Floman does teach that the memory controller (ASIC) is used to communicate between a processor and memory (Page 1, Paragraph [0004]). However, Yip teaches a system on a chip that includes both a memory controller and a processor (Figure 3). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included a processor as taught by Yip on the chip as taught by Floman in order to simplify the computer system by reducing separate components.

26. As for Claim 19, Floman also teaches the limitation that separate control lines are always maintained.

27. As for Claim 20, it is inherent that a processor is a state machine.

28. As for Claim 21, Floman and Yip do not teach configuring the hardware circuit using a graphical user interface. OFFICIAL NOTICE is taken that hardware is routinely configured under a graphical user interface such as Windows 95/XP through such items as the registry or control panel. It would have been obvious to one of ordinary skill in the art at the time of the invention to have configured the controller of Floman and Yip using a graphical user interface in order to make configuration intuitive.

29. As for Claim 23, the examiner takes OFFICIAL NOTICE that SDRAM and SRAM are common tri-state devices accessible by a memory controller, and as such It would have been obvious to one of ordinary skill in the art at the time of the invention to have included them in the tri-state devices accessible by the memory controller of Floman and Yip.

30. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Floman and Yip as applied to claim 2 above, and further in view of U.S. Patent No. 4,644,494 ("Muller"). Floman and Yip teach all of the limitations inherited from Claim 1, but they do not teach the use of shared address and data lines (Column 8, Lines 44-56). However, Muller teaches a system in which the address and data signals can be sent on shared lines. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the shared lines taught by Muller in the system of Floman and Yip in order to simplify the circuit by reducing signal lines.

31. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Floman and Yip as applied to claim 17 above, and further in view of U.S. Patent No. 6,801,459 ("Riesenman" et al.). Floman and Yip teach all of the limitations inherited from Claim 17, but they do not teach that the I/O lines comprise data mask lines. However, Riesenman teaches that a set of signals transmitted by a memory controller comprises data-masking signals (Column 3, Lines 36-54). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included these signals in the signal lines of Floman and Yip in order to increase the functionality of the system.

32. Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Floman and Yip as applied to claims 17 and 23 above, and further in view of U.S. Patent No. 5,875,470 ("Dreibelbis" et al.).

33. As for Claim 24, Floman and Yip teach all of the limitations inherited from Claims 17 and 23, but they do not teach that the SDRAM is arranged in multiple banks with independent row address management. However Dreibelbis does teach the use of multiple banks of SDRAM with independent row addressing. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the addressing as taught by Dreibelbis in the system of Floman and Yip.

34. As for Claims 25-26, the limitations of the claims describe a burst transaction, which is taught by Dreibelbis in Column 10, Lines 40-61.

35. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Floman and Yip as applied to claim 1 above, and further in view of U.S. Patent No. 6,836,815 ("Purcell" et al.)

36. As for Claims 27-28, Floman and Yip teach all of the limitations inherited from Claim 1, but they do not teach the use of a simultaneous multiple primary component fabric coupling the processor core to the memory controller, allowing separate primary components to access separate secondary components concurrently. However, Purcell teaches the use of a crossbar switch network, that allows separate processors to access separate memory controllers (Figure 1; Abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included such a network in the system of Floman and Yip in order to increase the efficiency of the system.

37. As for Claim 29, the examiner takes OFFICIAL NOTICE that multiplexers are a common component of crossbar switch networks.

38. Claims 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0199741 ("Floman") in view of U.S. Patent No. 5,623,645 ("Yip" et al.). Floman teaches a memory controller with a plurality of signal pins (lines) operable to allow access to off-chip devices, wherein the memory controller is configured to use separate signal pins to access different off-chip devices (Figures 1 and 4; Page 3, Paragraphs [0031]-[0033] and [0039]). While Floman does not explicitly teach that a processor is also included on the chip, Floman does teach that the memory

controller (ASIC) is used to communicate between a processor and memory (Page 1, Paragraph [0004]). However, Yip teaches a system on a chip that includes both a memory controller and a processor (Figure 3). It would have been obvious to one of ordinary skill in the art at the time of the invention to have included a processor as taught by Yip on the chip as taught by Floman in order to simplify the computer system by reducing separate components.

39. Claims 5 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy S. Cerullo whose telephone number is (571) 272-3634. The examiner can normally be reached on Monday - Thursday, 8:00-4:00; Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JSC

PAUL R. MYERS
PRIMARY EXAMINER